A Five Day Workshop on High Performance VLSI Architectures for Digital Signal Processing

Date: 30 April to 04 May 2018
Venue: IIITDM Kancheepuram, Melakottaiyur, Vandalur-Kelambakkam Road, Chennai - 600 127

1 Objective

This workshop aims to provide hands on implementation of the high performance VLSI architectures for Digital Signal Processing blocks such as MAC, DFT, DWT, DCT and other orthogonal discrete transformations. Key parameters to be considered for designing the basic building blocks of the DSP are trained during the workshop. At the end of the workshop the participant will be in a position to design and develop hardware based IPs for DSP. This workshop will enable the researchers and students to solve various research problems related to VLSI Signal Processing architectures.

2 Organized By

Center for High Performance Reconfigurable Computing, Department of Computer Science and Engineering, Indian Institute of Information Technology Design and Manufacturing (IIITDM) Kancheepuram. IIITDM Kancheepuram is an Institute of National Importance under Ministry of Human Resources Development, Govt. of India. IIITDM Kancheepuram is established in the year 2007 with a vision to excel as a center for excellence in IT enabled Design and Manufacturing. This workshop is aligned to the vision statement of the Institute to develop the human resources in hardware based IP development for DSP.

3 Topics to be Covered

- Introduction to Digital Signal Processing, VLSI Architectures, Performance Parameters to be considered during design, Types of computing.
- Design of High Performance Adders and Multipliers.
- Design of High Performance MAC.
- Basic DSP blocks implementation – DCT, DWT, AFT and Other discrete orthogonal transforms.
- DSP Processor Architectures, Major block implementation Details and Computing using DSP processors.
- VLSI Signal Processing Research Challenges

4 Target Audience

Faculty/Scientists/Researchers/PG and UG Students working on High Performance DSP block implementation, hardware based signal, image and video processing systems implementation. Free Internship opportunity at HPRC will be given for the interested UG and PG student participants.

5 Prerequisite

Participant should have the working knowledge of digital logic systems and fundamental concepts related to signal and digital signal processing.

6 Registration Details

- Online Registration – Open from March 01, 2018.
- Registration will be on the first come first served basis.
- Register your seat at the earliest as the seats are limited.
- Registration Closes by April 15, 2018.

7 Registration Fees

R&D Labs/ Faculty/ PSUs	Rs. 7000*
Full Time or Part Time Research Scholars, PG & UG Students	Rs. 6000*

* Inclusive of 18% GST as per GoI norms.

8 Important Details

- Please register for the workshop on the following Link: http://web.iiitdm.ac.in/noor/
- Details of mode of Payment and RTI information are available on the registration Page for the workshop.
- Registration Fee covers FOOD and ACCOMMODATION for all the 5 days. No TA/DA will be provided.
- DD should reach us on or before April 25, 2018 to the following address.

Dr Noor Mahammad Sk
Workshop Organizing Chair,
DSP Architecture Workshop
Indian Institute of Information Technology,
Design and Manufacturing (IIITDM) Kancheepuram
Melakottaiyur, Vandalur – Kelambakkam Road,
Chennai – 600 127, Tamil Nadu, India.

For enquiry and clarification, please contact:
Email: noorse@gmail.com; 044-2747 6349/ 91760 10587(M)

How to Reach Venue (www.iiitdm.ac.in):
IIITDM Kancheepuram Campus in Chennai on Vandalur – Kelambakkam Road. It is 9KMs from Vandalur Zoo toward East Direction, Landmark: KANDIGAI.