

# A Five Day Workshop on High Performance VLSI Architectures for Digital Signal Processing

Date: 10 TO 14 JUNE 2019

Venue: @IIITDM Kancheepuram, Melakottaiyur, Vandalur-Kelambakkam Road, Chennai - 600 127

## 1 Objective

This workshop aims to provide hands on implementation of the high performance VLSI architectures for Digital Signal Processing blocks such as adders, Multipliers, MAC, DFT, DWT, DCT and other orthogonal discrete transformations. Key parameters to be considered for designing the basic building blocks of the DSP are trained during the workshop. At the end of the workshop the participant will be in a position to design and develop hardware based IPs for DSP. This workshop will enable the researchers and students to solve various research problems related to VLSI Signal Processing architectures.

## 2 Organized By

Center for High Performance Reconfigurable Computing, Department of Computer Science and Engineering, Indian Institute of Information Technology Design and Manufacturing (IIITDM) Kancheepuram. IIITDM Kancheepuram is an Institute of National Importance under Ministry of Human Resources Development, Govt. of India. IIITDM Kancheepuram is established in the year 2007 with a vision to excel as a center for excellence in IT enabled Design and Manufacturing. This workshop is aligned to the vision statement of the Institute to develop the human resources in hardware based IP development for DSP.

## 3 Topics to be Covered

- Introduction to Digital Signal Processing, VLSI Architectures, Performance Parameters to be considered during design, Types of computing.
- Design of High Performance Adders and Multipliers.
- Design of High Performance MAC.
- Basic DSP blocks implementation DCT, DWT, AFT and Other discrete orthogonal transforms.
- DSP Processor Architectures, Major block implementation Details and Computing using DSP processors.
- VLSI Signal Processing Research Challenges
- Approximate Computing

## 4 Target Audience

Faculty/Scientists/Researchers/PG and UG Students working on High Performance DSP block implementation, hardware based signal, image and video processing systems implementation. Free Internship opportunity at HPRC will be given for the interested UG and PG student participants.

## 5 Prerequisite

Participant should have the working knowledge of digital logic systems and fundamental concepts related to signal and digital signal processing. Basic understanding of VLSI Design.

## 6 Background of Previous Events

CHRC has very good expertise in organizing the workshop in a well planned manner. The details of the previous workshops, budget and feedback from the participant can be found at <http://web.iiitdm.ac.in/noor/athprcse.html>

## 7 Registration Details

- Online Registration Open from April 10, 2019.
- Registration Link:  
<http://web.iiitdm.ac.in/noor/index.html>
- Registration Closes by June 08, 2019.

## 8 Registration Fees

R&D Labs/ Faculty/ PSUs With Hostel Accommodation	Rs. 8000*
R&D Labs/ Faculty/ PSUs Without Accommodation	Rs. 6000*
Research Scholars, PG & UG Students with Accommodation	Rs. 7000*
Research Scholars, PG & UG Students without Accommodation	Rs. 6000*

\* Inclusive of 18% GST as per GoI norms and 15% Institute Overheads.

## 9 Important Details

- NEFT or IMPS Account Details:  
IIITDM Educational Events; Acc.No:35594334673;  
State Bank of India; Kandigai Branch; IFSC  
code: SBIN0018365.
- Registration Fee covers FOOD and HOSTEL ACCOMMODATION for all the 5 days. No TA/DA will be provided.

## 10 Contact Info:

**Dr Noor Mahammad Sk & Dr Sree Hari V**

Workshop Organizing Chair  
DSP Architecture Workshop  
Indian Institute of Information Technology,  
Design and Manufacturing (IIITDM) Kancheepuram  
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**For enquiry and clarification, please contact:**

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**How to Reach Venue ([www.iiitdm.ac.in](http://www.iiitdm.ac.in)):**

IIITDM Kancheepuram Campus in Chennai on Vandalur Kelambakkam Road. It is 9KMs from Vandalur Zoo toward East Direction, Landmark: KANDIGAI.