A Five Day Workshop on High Performance Packet Processing Algorithms and Architectures

Date: 14 May to 18 May 2018
Venue: IIITDM Kancheepuram, Melakottaiyur, Vandalur-Kelambakkam Road, Chennai - 600 127

1 Objective

This workshop will provide an excellent opportunity to students, researchers and practitioners to attend the in depth lectures on the packet processing algorithms and architectures. This workshop will provide hands on implementation of the few packet processing algorithms and its performance estimations will be demonstrated. To enhance the knowledge and understandings on the packet processing, we plan to give a few demonstrations of the various works related to packet processing.

2 Organized By

Center for High Performance Reconfigurable Computing, Department of Computer Science and Engineering, Indian Institute of Information Technology Design and Manufacturing (IIITDM) Kancheepuram. IIITDM Kancheepuram is an Institute of National Importance under Ministry of Human Resources Development, Govt. of India. IIITDM Kancheepuram is established in the year 2007 with a vision to excel as center for excellence in IT enabled Design and Manufacturing. This workshop is aligned to the vision statement of the Institute to develop the human resources for enhancing the speed requirements of packet processing.

3 Topics to be Covered

- Introduction to network algorithmics, Network bottlenecks.
- Network Implementation Models.
- Principles to improve the performance of the network systems.
- Endnodes architectures and its performance limitations.
- Demultiplexing and protocol processing.
- Router architectures and algorithms.

4 Target Audience

Faculty/Scientists/Researchers/PG and UG Students working on network systems and network protocols. Free Internship opportunity at HPRC will be given for the interested UG and PG student participants.

5 Prerequisite

Participant should have working knowledge of data structures and algorithms, and fundamental concepts about computer organization and computer networks.

6 Registration Details

- Online Registration – Open from March 01, 2018.
- Registration will be on the first come and first serve basis.
- Register your seat at the earliest as the seats are limited.
- Registration Closes by May 10, 2018.

7 Registration Fees

R&D Labs/ Faculty/ PSUs	Rs. 7000*
Full Time or Part Time Research Scholars, PG & UG Students	Rs. 6000*

* Inclusive of 18% GST as per GoI norms.

8 Important Details

- Please register for the workshop on the following Link: http://web.iiitdm.ac.in/noor/
- Details of mode of Payment and RTI information are available on the registration Page for the workshop.
- Registration Fee covers FOOD and ACCOMMODATION for all the 5 days.
- No TA/DA will be provided.
- DD should reach on or before May 10, 2018 to the following address.

Dr Noor Mahammad Sk
Workshop Organizing Chair,
High Performance Packet Processing Workshop
Indian Institute of Information Technology,
Design and Manufacturing (IIITDM) Kancheepuram
Melakottaiyur, Vandalur - Kelambakkam Road,
Chennai - 600 127, Tamil Nadu, India.

For enquiry and clarification, please contact:
Email: noorse@gmail.com; 044-2747 6349/ 91760 10587(M)

How to Reach Venue (www.iiitdm.ac.in):
IIITDM Kancheepuram Campus in Chennai on Vandalur - Kelambakkam Road. It is 9KMs from Vandalur Zoo toward East Direction, Landmark: KANDIGAI.